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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte FRANCESCO A. CAMPISANO, DENNIS P. CHENEY,
and DAVID A. HRUSECKY

Appeal 2009-003334
Application 10/079,651
Technology Center 2600

Decided: September 23, 2009

Before KENNETH W. HAIRSTON, JOHN C. MARTIN,
and MAHSHID D. SAADAT, *Administrative Patent Judges*.

SAADAT, *Administrative Patent Judge*.

DECISION ON APPEAL

Appellants appeal under 35 U.S.C. § 134(a) from a Final Rejection of claims 1-5, 7-12, 14, and 15. Claims 6 and 13 have been objected to by the Examiner for being dependent on rejected claims, but otherwise allowable if rewritten in independent form to include all the limitations of their base

claim and those of any intervening claims. We have jurisdiction under 35 U.S.C. § 6(b).

We affirm-in-part.

STATEMENT OF THE CASE

Invention

Appellants' invention relates to decoding of digital motion video signals with low latency and minimal memory capacity requirements while high quality and arbitrary scaling and positioning are achieved (Spec. 1:8-11). According to Appellants, a frame switch point in accordance with a signal corresponding to completion of decoding of a previous frame is determined (Spec. 11:24-27). Then the motion video decoder is synchronized with a bottom border of a scaled image (Spec. 11:27-28).

Claims 1 and 9 are illustrative of the claimed invention and read as follows:

> 1. A method of operating a motion video decoder for decoding compressed image data, said method including steps of
>
> determining a frame switch point in accordance with a signal corresponding to completion of decoding of a previous frame, and
>
> synchronizing said motion video decoder for decoding compressed image data in accordance with one of display of a bottom border of a scaled image and said frame switch point.
>
> 9. A method of operating a motion video decoder comprising steps of
>
> testing spill buffer capacity responsive to a signal to produce a test result, and

controlling scaling in a decoding path of a decoder and altering decoder latency in response to said test result.

References

The prior art applied in rejecting the claims on appeal is:

Cheney	US 5,668,599	Sep. 16, 1997
Simmons	US 7,006,588 B2	Feb. 28, 2006 (filed Nov. 28, 2001)

Rejections

Claim 1 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Simmons.

Claims 2-5, 7-12, 14, and 15 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Simmons in view of Cheney.

We refer to the Briefs (Appeal Brief filed Oct. 1, 2007 and Reply Brief filed March 3, 2008) and the Answer (mailed Jan. 2, 2008) for their respective details. Only those arguments actually made by Appellants have been considered in this decision. Arguments which Appellants did not make in the Briefs have not been considered and are deemed waived. *See* 37 C.F.R. § 41.37(c)(1)(vii).

ISSUES

35 U.S.C. § 103 Rejection over Simmons

With respect to claim 1, the Examiner relies on frame synchronization (FS) of Simmons as suggesting the transition between images or frames to meet the claimed step of synchronizing the decoder in accordance with the frame switch point (Ans. 3). Appellants argue that the FS in Simmons precedes data for a frame and cannot correspond to completion of decoding

of a previous frame or serve to indicate when decoding of a received frame can begin (App. Br. 19-20). Appellants further assert that the FS pattern of Simmons does not indicate a point in time, rather, it is a location in a code stream indicating the beginning of the code for a frame (App. Br. 20). Therefore, the arguments made by Appellants present us with the following first issue:

1. Have Appellants shown that the Examiner erred in rejecting claim 1 under 35 U.S.C. § 103(a) by modifying Simmons to specifically teach the claimed step of synchronizing the decoder in accordance with the frame switch point?

35 U.S.C. § 103 Rejection over Simmons and Cheney

With respect to the rejection of claims 2-5, 7-12, 14, and 15, the Examiner relies on Cheney for teaching a spill buffer and altering the decoding latency by holding back the decoding (Ans. 4). Appellants specifically argue that the combination of the references does not teach all the recited features of independent claim 9 because Cheney does not relate to scaling or positioning of the image on the display (App. Br. 22). Appellants further argue that Cheney only determines if an address exceeds the capacity of another buffer, instead of testing the spill buffer (App. Br. 23). Regarding the rejection of the remaining dependent claims, we note that Appellants merely provide general assertions that Cheney does not disclose the specific recited features of these claims (App. Br. 24-26). Therefore, we select claim 9 as representative of the claims on appeal that are rejected over Simmons and Cheney. *See* 37 C.F.R. § 41.37(c)(1)(vii).

Thus, the arguments made by Appellants present us with the following second issue:

2. Have Appellants shown that the Examiner erred in rejecting claims 2-5, 7-12, 14, and 15 under 35 U.S.C. § 103(a) by combining Simmons and Cheney to specifically teach the claimed steps of testing the spill buffer capacity, controlling scaling in a decoder path and altering the decoder latency in response to the test?

FINDINGS OF FACT

The following findings of fact (FF) are relevant to the issues involved in the appeal.

Simmons

1. Simmons discloses a system and method for detecting a synchronization (sync) signal in a communication signal such that when a detected sync signal is determined to be invalid, previously read portions of the received communication signal, preferably beginning at a portion of the received signal immediately after a start of the detected sync signal, are again read and monitored to detect the sync signal. (Abstract.)

2. As shown in Figure 3, Simmons discloses a frame structure that includes frame 60 having a frame head 62 and a data portion 64. The frame head includes a sync signal in the form of the frame synchronization (FS) pattern 66. (Col. 5, ll. 13-17.)

3. The FS pattern 66 is a data or bit pattern that determines frame timing and other synchronization information by a receiver. (Col. 5, ll. 21-25.)

4. As shown in Figure 4, a timing diagram shows the operation of a sync signal detector by the receiver 50 during which the received data is monitored to detect the stream 70 for an FS pattern, referred to hereinafter as

simply an FS. Once the FS 72 is detected in the data stream 70, the receiver is synchronized to enter the decode state and decode a complete frame of data. (Col. 5, ll. 38-49.)

Cheney

5. Cheney discloses a digital signal decoder system that receives compressed encoded digitized video signals and transmits decompressed decoded digital video signals requiring a minimum of DRAM demand through the use of a Spill Buffer. (Abstract.)

6. Based on the MPEG-2 Standard, Cheney uses Variable Length Code Decoder, Inverse Quantizer, and Inverse Discrete Cosine Transform Decoder in addition to the conventional Discrete Cosine Transform with weighted scalar quantization to achieve high levels of video compression. (Col. 3, ll. 8-17; col. 5, ll. 5-24.)

7. As shown in Figure 5, Cheney provides for a Motion Compensation Unit 341 that receives dequantized signals from the Dequantizer Unit 321 and performs the required interpolations to form predicted blocks. By this summation step, these blocks are synchronized to the output of the Inverse Discrete Cosine Transform and added to the output of the Inverse Discrete Cosine Transform reconstructed block. (Col. 9, l. 66 – col. 10, l. 5.)

8. In discussing Frame Buffer Management, Cheney discloses that as frames are decoded, they are placed into one of the three logical frame buffers; Reference Frames, I, or P frames. The decoding process assigns the buffer dynamically to the frame being decoded. No reference frames are necessary in order to decode an I frame. One reference frame is required in order to decode a P frame because of the forward motion vectors. Two

Reference frames are required in order to decode a B frame. This is due to the existence of both forward and backward motion vectors. (Col. 14, ll. 7-16.)

9. The existence of B Frames creates a situation where the decoded frames are not received in display order, allowing time to decode both the past reference frame and the future reference frame before decoding the B Frame. In order to minimize memory size, successive B frames must reuse a portion of the same area in memory in order to maintain the DRAM configuration to within 2 MBytes and reduce costs. The Spill Buffer, which is used to accomplish this task, is an overflow buffer that is dynamically assigned to one of the three buffers. (Col. 14, ll. 17-28.)

10. Using a buffer size register and a spill size register, hardware automatically detects whether a buffer's logical address exceeds the buffer size and steers the address to point at the Spill Buffer. (Col. 14, ll. 28-36.)

11. After decoding one B frame, the Spill Buffer allows the decoding to begin on the second B frame while the first B frame is being displayed while providing some spacing between the two processes, *so that they do not run into each other*. In the event that the decode process is fast, a hardware interlock *will hold back the decoding* until the display process is beyond the point of conflict. (Emphasis added.) (Col. 14, ll. 37-44.)

12. Picture 1 is loaded starting at the beginning of the frame buffer at index=i1, which is adjusted to i2 for Picture 2 to begin at a location immediately following picture 1. Since picture 1 totally filled the frame buffer, picture 2 is loaded at the beginning of the Spill Buffer, and wraps around to the beginning of the frame buffer to complete its decoding. Similarly, picture 3 begins immediately following picture 2. Hardware

senses when the frame buffer boundary is reached in real storage, and automatically adjusts the real address to point to the top of the Spill Buffer to continue decoding. (Col. 14, ll. 54-63.)

13. As depicted in Figure 15, the capacity of the spill buffer is set to a value that is less than the maximum allocated area for the frame buffer and is shown as smaller than half the data field in each frame buffer. (Col. 15, ll. 4-31.)

PRINCIPLES OF LAW

In rejecting claims under 35 U.S.C. § 103, "the examiner bears the initial burden, on review of the prior art or on any other ground, of presenting a *prima facie* case of unpatentability." *In re Oetiker*, 977 F.2d 1443, 1445 (Fed. Cir. 1992). The test for obviousness is what the combined teachings of the references would have suggested to one of ordinary skill in the art. *See In re Kahn*, 441 F.3d 977, 987-88 (Fed. Cir. 2006); *In re Young*, 927 F.2d 588, 591 (Fed. Cir. 1991); *In re Keller*, 642 F.2d 413, 425 (CCPA 1981). Further, a rejection based on § 103 must rest upon a factual basis rather than conjecture or speculation. "Where the legal conclusion [of obviousness] is not supported by facts it cannot stand." *In re Warner*, 379 F.2d 1011, 1017 (CCPA 1967). *See also Kahn*, 441 F.3d at 988.

> Section 103 forbids issuance of a patent when "the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains."

KSR Int'l Co. v. Teleflex Inc., 550 U.S. 398, 406 (2007).

Such a showing requires

> 'some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness' . . . [H]owever, the analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ.
>
> *Id*. at 418 (quoting *Kahn*, 441 F.3d at 988).

ANALYSIS

35 U.S.C. § 103 Rejection over Simmons

In rejecting claim 1, the Examiner characterizes using frame synchronization (FS) pattern as the step of synchronizing in accordance with the frame switch point (Ans. 5). The Examiner concludes (*id.*) that FS pattern indicates a point where different frames occur or frames are switched since Simmons, upon detection of the FS pattern, enters a decode state and completely decodes a data frame.

We disagree with the Examiner's characterization of the FS pattern as the claimed frame switch point. As asserted by Appellants (App. Br. 19), the claimed determining a frame switch point based on a signal that corresponds to decoding a previous frame cannot be performed based on a signal that precedes data for a frame with no temporal relation to a previous frame. In that regard, Simmons discloses that the received signal starts after a detected sync signal (FF 1) is received in the form of a frame synchronization (FS) pattern included in the frame head (FF 2) for determining frame timing and synchronization information (FF 3). At the time of detecting the FS pattern, the receiver of data synchronizes and starts decoding (FF 4). In other words, the sync signal in Simmons is a forward

looking point, and not a point marking the "completion of decoding of a previous frame," as recited in claim 1.

We also agree with Appellants (App. Br. 20) that the FS pattern of Simmons is included in the frame header and marks a location in a code stream, which is different from the claimed frame switch point and is determined based on completion of decoding a previous frame. Whereas, the Examiner's position relies on identifying a point where different frames occur (Ans. 5), but is actually based on the next frame. As argued by Appellants (Reply Br. 3), the time of detection of the FS pattern in Simmons does not correspond to the time of completion of decoding a previous frame since at that point, the search for the next FS pattern has started (*See* FF 4). Thus, the 35 U.S.C. § 103(a) rejection of claim 1 over Simmons cannot be sustained.

35 U.S.C. § 103 Rejection over Simmons and Cheney

1. *Claims 2-5, 7, and 8*

Claims 2-5, 7, and 8 depend from claim 1, which as discussed above, recites features that are not suggested by Simmons. Additionally, we find that the Examiner has not identified any teachings in the secondary reference related to the claimed step of synchronizing the decoder in accordance with the frame switch point to overcome the deficiencies of Simmons discussed above. Therefore, we do not sustain the 35 U.S.C. § 103 rejection of claims 2-5, 7, and 8 over Simmons and Cheney.

2. *Claim 9*

With respect to claim 9, Appellants argue that Cheney does not teach

or suggest testing the spill buffer and merely determines if an address exceeds the capacity of another buffer to which the spill buffer may be assigned to avoid collision of data (App. Br. 23). We disagree, since Cheney actually "tests" the spill buffer capacity by such determination (FF 8-10). As stated by the Examiner (Ans. 6), the hardware would have to perform a test to determine if the buffer size has been exceeded.

We also agree with the Examiner's line of reasoning (Ans. 6) that holding back the decoding in Cheney is the same as altering the decoder latency. Contrary to Appellants' assertion (App. Br. 23; Reply Br. 4) that there is no change in latency to any test in Cheney, but only a delay provided when decoding is completed early, the reference discloses that the spill buffer is an overflow buffer used in decoding (FF 10). Cheney, in fact, starts decoding the second B frame as the first B frame is being displayed while some delay of the decoding avoids conflict of frames in the display process (FF 11). We also agree with the Examiner (Ans. 6) that the claimed "controlling scaling in a decoding path" and "altering decoder latency" read on wrapping the logical addresses that reconfigures the frame buffer and on holding back decoding in Cheney (FF 11-12). Thus, the 35 U.S.C. § 103(a) rejection of claim 9 over Simmons and Cheney is sustained since Appellants have not shown error in the Examiner's position.

3. Claim 10

Appellants argue (App. Br. 24) that Cheney does not teach or suggest reconfiguring the frame buffer for the purpose of accommodating an increased latency. As discussed above and stated by the Examiner (Ans. 6), wrapping the logical address in Cheney reconfigures the frame buffer while the decoding is held back in order to provide some spacing between the

decoding processes (FF 11-12). Such reconfiguration of addresses meets the claimed reconfiguring a frame buffer for accommodating an increased latency.

4. Claim 11

Appellants again merely challenge the Examiner's position by repeating the claim limitation and contending that the limitation is missing in the combination of the references (App. Br. 24-25). The Examiner also appropriately refers to using scalar quantization in Cheney that is used for decoding video data in the MPEG-2 Standard in a continuous manner (Ans. 7). We agree with the Examiner and find that Cheney does disclose using various scalar quantizations to achieve video compression (FF 7) based on the MPEG-2 Standard (FF 6). Therefore, the disclosed scaling of the video data in Cheney is continuous since applying MPEG-2 Standard implies decoding continuous frame of a motion video which meets the claimed "continuously scaling" of the data.

5. Claim 12

Appellants argue that the portions of Cheney relied on for teaching performing the scaling step by interpolation is directed to "interpolation to form predicted image blocks" (App. Br. 25). We disagree and find that the Examiner has properly relied (Ans. 4) on decoding the predicted blocks that are formed using interpolation (FF 7). These Predicted blocks or P frames are disclosed in Cheney to involve wrapping the logical address that changes or scales the frame buffer by interpolation (FF 8-9).

6. Claims 14 and 15

We again disagree with Appellants (App. Br. 25-26) that the capacity of the spill buffer, while taught by Cheney to be less than half of the field, is

fixed and cannot be scaled or reconfigured. We are not persuaded since, even if the spill size may have a maximum capacity (FF 13), the scaling of the spill buffer in Cheney involves adjusting the logical address that points to the locations in the spill buffer (FF 10-13).

CONCLUSION

In view of our analysis above, we find that Appellants have shown that the Examiner erred in rejecting claim 1 under 35 U.S.C. § 103(a) by modifying Simmons to specifically teach the claimed step of synchronizing the decoder in accordance with the frame switch point. Therefore, the 35 U.S.C. § 103(a) rejection of claims 1, as well as claims 2-5, 7, and 8 dependent upon claim 1, over the combination of Simmons and Cheney cannot be sustained.

However, Appellants have not shown that the Examiner erred in rejecting claim 9 under 35 U.S.C. § 103(a) by combining Simmons and Cheney to specifically teach the claimed steps of testing the spill buffer capacity, controlling scaling in a decoder path and altering the decoder latency in response to the test. Thus, we sustain the 35 U.S.C. § 103(a) rejection of independent claim 9, as well as claims 10-12, 14, and 15 dependent thereon and shown *supra* to have limitations that are taught or suggested by the combination of Simmons and Cheney.

ORDER

The decision of the Examiner rejecting claims 9-12, 14, and 15 is affirmed, but reversed with respect to claims 1-5, 7, and 8.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. 1.136(a)(1)(iv).

AFFIRMED-IN-PART

gvw

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